

REMARKS/ARGUMENTS

The present amendment is submitted in response to the Office Action received from the United States Patent Office dated June 8, 2009. The Patent Office rejected Claims 1-11 under 35 U.S.C. §102(e) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681).

In response to the Office Action, Applicant respectfully requests that the Examiner reconsider the rejections. However, the Applicant has amended Claim 1 and Claim 7 to overcome the Examiner's rejections. Applicant respectfully submits that the amendments and the explanations below overcome the rejections to the claims. Applicant submits that all of the claims are now in condition for allowance. Notice to that effect is requested.

The Patent Office rejected Claims 1-11 under 35 U.S.C. §102(e) as being anticipated by *Hovell et al.* (U.S. Patent Number 7,116,681). The Patent Office states that Claim 1, *Hovell et al.* discloses a communication protocol converter comprising: (a) a first modular communication jack having: i) a housing defining an open cavity and a segregated interior chamber; ii) a connector port having a plurality of electrical contacts positioned within said open cavity; iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a first communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port; where in the circuitry components are positioned on both sides of the at least one circuit board (Ports connecting 62(A, B) and 72 (A, B) of fig. 2, col. 8 line 10 to col. 9 line 20); and iv) a memory positioned on said circuit board in electrical communication with said conversion circuitry for a first communication protocol for receiving converted data (using network controller to process data conversion, see figs.1, 2, col.6 line 13 to col.7 line 50); whereby the memory is interconnected to a bi-directional data line that allows the input and output of data (writing and accessing data from/to the storage (68A fig.2), see col.8 line 10 to col.9 line 20) 0(b) a second modular communication jack having: i) a housing defining an open cavity and a segregated interior chamber; ii) a connector port having a plurality of electrical contacts positioned within said open cavity; iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a second communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port; iv) a memory positioned on said circuit board in electrical

communication with said conversion circuitry for said second communication protocol for receiving converted data (see fig.2, col.7 line 17 to col.8 line 58) wherein the memory is connected with the bi-directional line to receive input of raw data from the first modular communication jack; and (c) a bidirectional data interface electrically interconnecting said memory of said first communication jack with said memory of said second communication jack (processing data in/out of the storage, see col.8 lines 10-58).

The Patent Office states as to Claim 7, *Hovell et al.* discloses a communication protocol converter comprising: a housing defining first and second open cavities and a segregated interior chamber; each of said open cavities incorporating a plurality of electrical contacts positioned within said open cavities to form first and second connector ports wherein said first connector port is adapted to interface with a first communication protocol and said second connector port is adapted to interface with a second communication protocol (using network controller to process data conversion, see figs. 1, 2, col.6 line 13 to col.7 line 50); and at least one circuit board incorporating communication protocol conversion circuitry components disposed within said interior chamber in electrical communication with the electrical contacts of said first and second connector ports wherein said conversion circuitry bi-directionally translates communication protocols (network protocol translation, see fig.2, col.7 line 17 to col.8 line 58), wherein the housing allows for the at least one circuit board to electronically communicate with both the first connector port and the second connector port and a microprocessor employing embedded software that converts Ethernet data from internet protocol version 4 to internet protocol version 6 (converting data from IPV4 to IPV6, see fig. 2, col. 7 line 17 to col.8 line 58).

Hovell et al. discloses a tunnel is established across an IPv4 domain for the transport of packets from a source host on one IPv6 domain to a destination host on another IPv6 domain, there being respective interfaces between the IPv4 domain and the IPv6 domains.

Amended Claim 1 requires a communication protocol converter having a first modular communication jack having: a housing defining an open cavity and a segregated interior chamber; a connector port having a plurality of electrical contacts positioned within said open cavity; at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a first communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port wherein the circuitry components are positioned on both sides of the at least one circuit board; and a memory

positioned on said circuit board in electrical communication with said conversion circuitry for a first communication protocol for receiving converted data whereby the memory is interconnected to a bi-directional data line that allows the input and output of raw data. The converter also has a second modular communication jack having: a housing defining an open cavity and a segregated interior chamber; a connector port having a plurality of electrical contacts positioned within said open cavity; at least one circuit board incorporating Ethernet to raw data conversion circuitry components for a second communication protocol disposed within said interior chamber in electrical communication with the electrical contacts of said connector port; a memory positioned on said circuit board in electrical communication with said conversion circuitry for said second communication protocol for receiving converted data wherein the memory is interconnected with the bi-directional line to receive input of raw data from the first modular communication; a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, said microprocessor utilizing embedded software to manipulate the data signal to provide data to magnetics; and a bidirectional data interface electrically interconnecting said memory of said first communication jack with said memory of said second communication jack.

Amended Claim 7 requires a communication protocol converter comprising: a housing defining first and second open cavities and a segregated interior chamber; each of said open cavities incorporating a plurality of electrical contacts positioned within said open cavities to form first and second connector ports wherein said first connector port is adapted to interface with a first communication protocol and said second connector port is adapted to interface with a second communication protocol; and at least one circuit board incorporating communication protocol conversion circuitry components disposed within said interior chamber in electrical communication with the electrical contacts of said first and second connector ports wherein said conversion circuitry bidirectionally translates communication protocols wherein the housing allows for the at least one circuit board to electronically communicate with both the first connector port and the second connector port; a microprocessor employing embedded software that receives Internet protocol 4 Ethernet data; removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data.

Hovell et al. does not teach or suggest a microprocessor employing embedded software that receives Internet protocol 4 Ethernet data; removes the Internet protocol 4 header data, inserts Internet protocol 6 header data, recalculates the necessary Internet protocol header fields and outputs corresponding Internet protocol 6 Ethernet data as required by Claim 7. On the contrary, *Hovell et al.* only discloses a general tunneling technique including either manual configuration of the tunneling technique or some sort of automation. (not specified). *Hovell et al.* does not teach a controller block in the form of a microprocessor which handles all the conversion between raw data and Ethernet, including processing of digital and analog signals, as well as all of the required code protocol translations, whereby the microprocessor utilizing embedded software to manipulate the data signal as required by Claim 1.

Further, Applicant notes that the Examiner does not point to any particular part of *Hovell et al.* that teaches any of the specific structural elements taught in the instant application. For example, the Patent Office states that *Hovell et al.* teaches a first and second modular communication jack having: i) a housing defining an open cavity and a segregated interior chamber; ii) a connector port having a plurality of electrical contacts positioned within said open cavity; iii) at least one circuit board incorporating Ethernet to raw data conversion circuitry components. However, the Patent Office illustrates these elements by pointing to Column 8, line 10 to column 9, line 20. The Patent Office does not illustrate the specific elements within those columns, nor does the Office specify which elements within those columns relates to the specific elements in the claims. The burden to show those elements is not on the applicant, but rather on the Examiner to show that the claims are in fact anticipated. Applicant should not be required to find those elements in the specification of a prior art reference.

Under 35 U.S.C. §102(e), anticipation requires that a single reference disclose each and every element of Applicant's claimed invention. *Akzo N.V. v. U.S. International Trade Commission*, 808 F.2d 1471, 1479, 1 USPQ 2d 1241, 1245 (Fed. Cir. 1986).

Moreover, anticipation is not shown even if the differences between the claims and the reference are "insubstantial" and one skilled in the art could supply the missing elements. *Structure Rubber Products Co. v. Park Rubber Co.*, 749 F.2d. 707, 716, 223 USPQ 1264, 1270 (Fed. Cir. 1984).

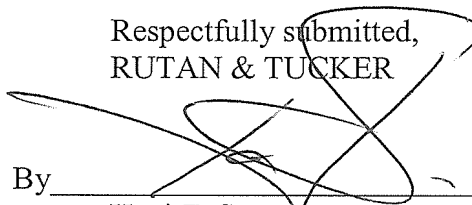
“A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.” *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (MPEP § 2131).

Applicant respectfully submits that this rejection overcomes based on the amendments to the independent claim for which this claim is based.

Claim 2-6 depend from Claim 1; Claims 8-11 depend from Claim 7. These claims are further believed allowable for the same reasons set forth with respect to independent Claims 1 and 7 since each sets forth additional novel steps of Applicant’s Communication Protocol Converter and Method of Protocol Conversion.

In view of the foregoing remarks, Applicant respectfully submits that all of the claims in the application are in allowable form and that the application is now in condition for allowance. any outstanding issues remain, Applicant urges the Patent Office to telephone Applicant’s attorney so that the same may be resolved and the application expedited to issue. Applicant requests the Patent Office to indicate all claims as allowable and to pass the application to issue.

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